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10/573,566	03/27/2006	Takeshi Ohtsuka	2006_0384A	4781
52349	7590	03/16/2009	EXAMINER	
WENDEROTH, LIND & PONACK L.L.P.			GIARDINO JR, MARK A	
1030 15th Street, N.W.				
Suite 400 East			ART UNIT	PAPER NUMBER
Washington, DC 20005-1503			2185	
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			03/16/2009	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/573,566	OHTSUKA, TAKESHI	
	<b>Examiner</b>	<b>Art Unit</b>	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 12 December 2008.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-5 and 7-12 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-3 and 7-12 is/are rejected.  
 7) Claim(s) 4 and 5 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date <u>7/17/2008</u> .	6) <input type="checkbox"/> Other: _____ .

**DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/19/2008 has been entered.

The Examiner acknowledges the applicant's submission of the amendment dated 11/19/2008. At this point, claims 1 and 12 have been amended and claim 6 has been cancelled. Thus, claims 1-5 and 7-12 are pending in the instant application.

The instant application having Application No. 10/573,566 has a total of 9 claims pending in the application, there are 2 independent claims and 9 dependent claims, all of which are ready for examination by the examiner.

**INFORMATION DISCLOSURE STATEMENT**

Applicant's argument regarding the IDS submitted 7/17/2008 have been considered and is persuasive. Accordingly, the information disclosure statement filed 7/17/2008 is being considered by the examiner.

**REJECTIONS BASED ON PRIOR ART**

*Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis et al (US 6,029,226) in view of Wallis (4,149,243).

**Regarding Claim 1**, Ellis ('226) teaches a drive device for writing data transmitted by a host device onto a memory card in accordance with a command issued by the host device, comprising:

a receiving unit operable to receive a plurality of commands issued by the host device (**"a first request is received"**, Column 3 Lines 24-31, **a receiving unit is inherently present because commands are received**); and

a writing unit operable, if a write end address of one of the received commands is consecutive with a write start address of a following command, to perform the data writing to the memory card by the consecutive commands in a single process (**see the "normal write" procedure described on Column 6 Lines 6-12 and, this "normal write" process can perform writes with consecutive addresses according to the claimed process as described below**); and

an analysis unit operable to decode the write-start address and a sector number of each command, the sector number being the number of sectors of data for writing the command (**such an analysis unit is inherently present to load the buffer with the sector numbers described in Column 5 Lines 33-40**);

the process involves processing to sequentially write data received from the host device to the memory card being repeated until a STOP instruction is given (**the status field “indicates a transfer has finished” [corresponding to a STOP instruction]**, **Column 5 Lines 54-58**),

the process is activated when the analysis unit decodes a write-start address A and the sector number s from the one command, and involves the data writing being started from the write-start address A (**the unit starts the write process as soon as it receives write information, Column 6 Lines 6-12, and inherently starts from a write address ‘A’ because there must be an address where the data is to be written to**),

the analysis unit analyzes the following command until the written sector number reaches s (**the analysis unit analyzes following commands [according to the receiving 600, storing 602, and parsing 604 analysis in Figure 6] even when the DMA engine is not ready [and presumably involved in a read or write transfer, note that after analyzing some commands, the microprocessor must wait until the DMA is ready as in Column 7 Lines 39-45]**).

However, Ellis does not teach wait commands. Wallis (US 4,149,243) teaches a command with an appended wait flag (**Column 11 Line 50-51 in Wallis**), where execution of commands are suspended until another command (“post signal”) is received (**Column 11 Line 67 to Column 12 Line 3 in Wallis**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have allowed commands to use the wait flags of

Wallis causing the analysis unit of Ellis to wait to coordinate execution of mutually dependent functions (**Column 2 Lines 38-46 in Wallis**).

**Regarding Claim 2**, Ellis ('226) and Wallis teach all limitations of Claim 1, wherein

an instruction unit operable to give the STOP instruction at a point when a written sector number reaches  $s + t$ , where  $s$  is the sector number of the one command and  $t$  is the sector number of the following command (Column 5 Lines 54-58, a status is given to indicate that a transfer has finished, since this appears to be done after all writes are finished, and this would include when the  $s + t$  sectors are written).

**Regarding Claim 3**, Ellis ('226) and Wallis teach all limitations of Claim 2, and the instruction unit gives the STOP instruction when the written sector number reaches  $s + t$ , if a write-start address  $B$  of the following command is consecutive with a write-end address  $A + s$  of the one command (Column 5 Lines 54-58, a status is given to indicate that a transfer has finished, since this appears to be done after all write processes are finished, and this would include when the  $s + t$  sectors are written).

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis ('226) and Wallis in view of Krantz (US 6,826,650).

**Regarding Claims 7 and 8**, Ellis ('226) and Wallis teach all limitations of Claim 3 as discussed above, but does not teach a tag attached thereto, with the flags showing an order of the commands. However, Krantz teaches a tag showing an order of the commands (see address registers and description Column 2 Lines 18-36 in Krantz). He

also teaches a storage unit operable to store commands received from the host device (buffer memory controller 230, also see Figure 1 in Krantz), a rearranging unit operable to rearrange the stored commands in order of the write-start addresses (such a unit is inherently present for the functionality described in Column 2 Lines 37-39 in Krantz) wherein the analysis unit performs the analysis in the rearranged order of the commands (such functionality is inherently present in the analysis unit for writing data on consecutive tracks as described in Column 2 Lines 33-36). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have provided the extra hardware functionality as listed above. Krantz provides the motivation when he states that adding these devices improves system performance (Column 2 Lines 41-52 in Krantz).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis ('226) and Wallis in view of Harari et al (US 5,297,148).

**Regarding Claim 9,** all limitations of Claim 2 have been discussed above. However, Ellis ('226) and Wallis do not teach an analysis unit that judges if the number of sectors is an integer multiple of the number of sectors in an erasable block of the memory card, and if the unit is judged in the negative, the instruction unit continues the process by not giving the STOP instruction even if the written sector number reaches  $s + t$ , and waits for a further command to be received. However, Oyaizu teaches a flash memory buffer that holds bytes of write information until it is ready to be written to a flash memory device (see Column 14 Line 41 to Column 15 Line 16 in Harari). It would

have been obvious to a person of ordinary skill in the art at the time the invention was made to have stored the write information in a buffer and wait until an integer multiple of the number of sectors were stored before acknowledging the STOP instruction from the host. As motivation, memory blocks are erased in block units and cannot be re-written without re-writing the entire contents of the block (see Column 4 Lines 44-49 in Harari). Therefore, a person having ordinary skill in the art would want to make sure that before writing to a block, as much data as possible is ready to be written to said block to avoid re-writing the block several times sequentially, thereby causing delays in write times. So, by combining the two devices, the additional benefit of faster write times is obtained.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis ('226) and Wallis in view of Carman et al (US 6,272,632).

**Regarding Claim 10**, this claim is the computer readable medium claim analogous to Claim 1 and is rejected under similar rationale.

However, Ellis ('226) and Wallis teach the functionality implemented in hardware. Carman teaches advantages of using software instead of hardware (Column 1 Line 53 to Column 2 Line 7 in Carman). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the device described by Ellis ('226) in software. As motivation, Carman lists the benefits of cost and ease of integration of software compared to hardware (Column 1 Line 53 to Column 2 Line 7 in Carman). Thus, by implementing the functionality in software, additional benefits are obtained.

**Regarding Claim 11**, this claim is the computer readable medium claim analogous to Claim 2, and since Carman renders changing hardware to software obvious, this claim is rejected under similar rationale as Claim 2.

**Regarding Claim 12**, this claim is the computer readable medium claim analogous to Claim 3, and since Carman renders changing hardware to software obvious, this claim is rejected under similar rationale as Claim 3.

## **ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

### ***Rejections - USC 102/103***

Applicant's arguments/amendments with respect to claims 1 and 10 that Ellis does not teach a wait flag has been considered and is persuasive, thus the Examiner's prior rejection has been withdrawn. However, new grounds of rejection have been made in light of a newly found prior art reference.

## **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

### **SUBJECT MATTER CONSIDERED ALLOWABLE**

Claims 4 and 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### **CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1-3 and 7-12 have received a second action on the merits and are subject of a second action final.

**DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino  
/M.G./

/Stephen Elmore/  
Primary Examiner, Art Unit 2185

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March 17, 2009